Curriculum Vitae 1

ARINDAM BANERJEE
E.MAIL:banerjee.arindam1@gmail.com
banerjeesobhana@gmail.com
Address:- Nibedita place, Taki Road,
P.O.Barasat, Dist:North 24-
Parganas,West Bengal,India,
Pin: 700124
Contact Number-9433279813/ 8902392467/
6290564216

EDUCATIONAL QUALIFICATION

YEAR	EXAM.	BOARD/ COUNCIL	MARKS(%)	CLASS/ DIVISION
2019	Ph.DCompleted in the Dept. of Computer Science and Engineering, Jadavpur University	Jadavpur University	-	-
2006-2008	M.TECH in VLSI and Microelectronics	M.A.K.A.U.T. (formerly known as W.B.U.T.)	78.7	1ST
2000-2004	B.E. in Electronics & Communication	BURDWAN UNIVERSITY	70	1ST
2000	Higher Secondary	W.B.C.H.S.E.	71.3	1ST
1998	Secondary	W.B.B.S.E.	85.3	1ST,*

Ph. D Thesis Title: Synthesis of Arithmetic Circuits in Conventional and Emerging Technologies
Ph. D Registration No.: 251/16/E Date: 03/05/2016

Publications related to Ph. D work: (3 Journals and 5 Conferences)

1. **A. Banerjee**, D. K. Das, "The design of reversible multiplier using ancient Indian mathematics", ISED-2013, pages-31-35, December, 2013, Singapore.
2. **A. Banerjee**, D. K. Das, "Squaring in reversible logic using iterative structure", East West Design and Test Symposium, 2014, Ukrain.
3. **A. Banerjee**, D. K. Das, "The Design of Reversible Signed Multiplier using Ancient Indian Mathematics", Journal of Low Power Electronics, vol. 11, October, 2015, pp. 467-478. (SCI(M), ScopusI.F. – 0.84)
4. **A. Banerjee**, D. K. Das, "A New Squarer Design with Reduced Area and Delay", IET Computers and Digital Techniques, vol. 10, issue 5, February, 2016, pp. 205-214. (SCI(E), I.F. – 0.515)
5. **A. Banerjee**, D. K. Das, "Squaring in Reversible Logic using Zero Garbage and Reduced Ancillary inputs", Int. Symp. On VLSI Design, January, 2016.
6. **A. Banerjee**, D. K. Das, "Squarer Design with Reduced Area and Delay", VLSI Design and Test Symp., May, 2015.
7. **A. Banerjee**, D. K. Das, "A New ALU Architecture Design using Reversible Logic", Int. Symp. On Electronic Design (ISED-2016), December, 2016.
8. **A. Banerjee**, D. K. Das, "A Novel ALU Circuitbased on Reversible Logic", Journal of Circuits, Systems and Computers, World Scientific Publisher, Vol. 29, No. 11, 15th September, 2020.(SCI)

Research Project Undergone: "Synthesis and Testing of Reversible Circuits in application to Nanotechnology and Quantum Computing", sponsored by CSIR, New Delhi, was performed in the Dept. of CSE, Jadavpur University under the supervision of Professor Debesh Kumar Das, HOD, Dept. of CSE, Jadavpur University from December, 2012 to November, 2014.

Other Publication:

1. **Arindam Banerjee**, "Detection and Elimination of Single and Multiple Missing Gate Fault(SMGF/MMGF) of Reversible Arithmetic Circuits", Power Devices and IoT for Intelligent System Design, Scrivener Publishing LLC, 2024, pp. 271-302 (proof reading).
2. **Arindam Banerjee**, "Analysis of Inheritance of Criminal Behavior from the Parents Using Genetic Algorithm", Smart Innovation, Systems and Technologies, chapter 30, vol. 405, Springer Nature, 2024.
3. **Arindam Banerjee**, Aniruddha Ghosh, Mainuck Das, "Design of A Novel Signed Binary Subtractor using Quantum Gates", Journal of Quantum Computing, Tech Science Press, vol. 4, no. 3, 2023.
4. **Arindam Banerjee**, "Optimized Test Pattern Generation for Single Missing Gate Fault Detection in Reversible Arithmetic Circuits", IEEE-EDKCON (International Conference)-2022,November, 2022.

5. **Arindam Banerjee**, Aniruddha Ghosh, Mainuck Das, SK Suman, Arvik Sai, "Memristor Based Multiplier and Squarer of some numbers of the form $10^l \pm m$", Journal of The Institution of Engineers (India): Series B (IEIB), vol. 103, pp. 1239–1247, 2022 (published, DOI: 10.1007/s40031-022-00717-7).

6. **Arindam Banerjee** and Debesh Kumar Das, "Arithmetic Circuits Using Reversible Logic: A Survey Report", Springer, LNCS. (Book chapter)

7. **A. Banerjee**, M. Das, A. Ghosh, "AI Based Online Data Segregation Method under COVID Situation", IOCER-2020, 8-9 October, 2020 (published in IOP (Journal of Physics – Conference Series)

8. **A. Banerjee**, S. Bhattacharyya, A. Deyasi, "High Speed Reconfigurable ALU Design for Radix ($2^n \pm m$)", Advances in Industrial Engineering and Management, American Scientific Publishers, vol. 5, no. 2, 2016, pp. 183-187, 2016. (ISSN: 2222-7059 (Print); E-ISSN: 2222-7067 (Online))

9. S. Pal, **A. Banerjee**, S. Bhattacharyya, "Optical Network Based RNS Multiplier in (2^n-1) Radix System using SOA-MZI", NCRAST-2016 at Heritage Institute of Technology.

10. **A. Banerjee**, S. Pal, S. Bhattacharyya, D. K. Das, "Memristor Based Modulo Multiplier Design For (2^n-1) and 2^n Radix", DevIC-2017, Kalyani Govt. Engineering College. (IEEE xplore)

11. **A. Banerjee**, S. Bhattacharyya, A. Deyasi, "Synthesis of High Speed Multi-valued ALU for ($2^n \pm m$) Radix", MCCS-2017, Ranchi. (Springer, Book chapter)

12. **A. Banerjee**, S. Bhattacharyya, A. Deyasi, "Fast Squaring Technique for Radix Vicinity Numbers for Radix ($2^n \pm m$) with reduced Computational Complexity", NCCS-2017, Ranchi. (Springer, Book chapter)

13. **A. Banerjee**, S. Pal, S. Bhattacharyya, D. K. Das, "Memristor Based MAC Architecture Design For (2^n-1) and 2^n Radix", Journal of Active and Passive Electronic Devices, Old City Publishing, Philadelphia, Vol. 0, pp. 1-19, 2017 (SCI(M), ISSN: 1555-0281 (print), ISSN: 1555-029X (online)).

14. **A. Banerjee**, A. Ghosh, M. Das, SK Suman, A. Sain, "Memristor Based Fast Decimal Squaring of some numbers of the form $10^l \pm m$", FEMAS-2019, October, 2019 (Accepted and Presented).

15. Prabir Kumar Saha, **Arindam Banerjee**, AnupDandapat, "High Speed Low Power Complex Multiplier Design Using Parallel Adders and Subtractors", International Journal on Electronic and Electrical Engineering, (IJEEE), Vol 07, No. 11 Page No. 38-46, 2009.

16. Prabir Kumar Saha, **Arindam Banerjee** and A. Dandapat ,"Low power and High Speed Factorial Design in 22nm Technology", accepted in AIP, 2010.

17. PrabirSaha, **A. Banerjee**, I. Banerjee and A. Dandapat, "High Speed Low Power Floating Point Multiplier Design Based on CSD (Canonical Sign Digit)"; Published in IJVED (National Journal).

18. P. Saha, **A. Banerjee**, A. Dandapat, P. Bhattacharyya, "Vedic Mathematics Based 32-Bit Multiplier Design for High Speed Low Power Processors"; Published in International Journal on Smart Sensing and Intelligent Systems.

19. Prabir Kumar Saha, **Arindam Banerjee**, A. Dandapat, P. Bhattacharyya, "ASIC design of a high speed low power circuit for factorial calculation using ancient Vedic mathematics", accepted in Microelectronics Journal, Elsevier.

20. **A. Banerjee**, M. Das, A. Ghosh, "FPGA Implementation of High Speed Numerically Controlled Oscillator for QAM architecture", accepted in National Conference NCACD to be held at HIT, Haldia, West Bemgal, August, 2012.

21. **A. Banerjee**, R. Ghosh, S. Ghosh, "High Performance Novel Square root architecture using Ancient Indian Mathematics for High Speed Signal Processing", accepted in National Conference NCACD to be held at HIT, Haldia, West Bemgal, August, 2012.

22.Prabir Saha, **Arindam Banerjee**, AnupDandapat and Partha Bhattacharya, "High Speed Vedic Multiplier for Decimal Number System"; accepted at VDAT-2012 organized by Bengal Engineering and Science University, 2012.

23. **Arindam Banerjee**, Atin Mukherjee and Debesh Choudhury, "VHDL Implementation of Spatial Fourier Processing", Accepted in ICONTOP-2012, held at Calcutta University, January, 2012.

24. **Arindam Banerjee**, Atin Mukherjee, Prabir K. Saha and Debesh Choudhury, "Computation of Fresnel Diffraction by VHDL", Accepted in FOP-11, held at IIT-Delhi, December, 2011.

25. Prabir Saha, **Arindam Banerjee**, Partha Bhattacharyya, AnupDandapat, "Vedic Divider: Novel Architecture (ASIC) for High Speed VLSI Applications"; accepted at ISED-2011 organized at Kochi.

26. Prabir Saha, **Arindam Banerjee**, Partha Bhattacharyya, AnupDandapat, "High Speed ASIC Design of Complex Multiplier Using Vedic Mathematics"; accepted at Techsym-2011 organized by IIT Kharagpur.

27. Prabir Saha, **A. Banerjee**, I. Banerjee and A. Dandapat, "High Speed Low Power Floating Point Multiplier Design Based on CSD (Canonical Sign Digit)"; IEEE symposium on VLSI Design and Testing, VDAT-2010, Accepted.

28. Prabir Saha, Ranjana Roy, Ishita Banerjee, **Arindam Banerjee**, "FPGA Implementation of 2D convolution Architecture using Wave-front Array"; national seminar on Recent Trends in Engineering and Technology Including Non-Conventional Energy" April 10, 2010 at IMPS, Malda.

29. Prabir Kumar Saha, **Arindam Banerjee** and A. Dandapat, "Low power and High Speed Factorial Design in 22nm Technology" accepted at ICANN-2009 conducted by IIT Guwahati.

Curriculum Vitae 3

WORK EXPERIENCE

Name of the organization	Department	From	To	Year of Experience	Nature of Responsibility	Position Held
JIS College of Engineering	Electronics and Communication Engineering	July, 2008	November, 2012	4 years 4 months	Teaching and Research	Assistant Professor
Jadavpur University	Computer Science and Engineering	December, 2012	November, 2014	2 years	Research in CSIR sponsored project	Research Associate
JIS College of Engineering	Electronics and Communication Engineering	December, 2014	December, 2022	7 years	Teaching and Research	Assistant Professor and Associate Professor (for last 07 months)
ICFAI University Tripura	ECE, Faculty of Science and Technology	January, 2023	November, 2024	1 year 10 months	Teaching and Research	Associate Professor
ADAMAS University	CSE, SOET	November, 2024	Till Date	1 month 20 days	Teaching and Research	Assistant Professor-III

Subjects Taught: - Basic Electronics, Analog Electronics, Digital Electronics, VLSI and Microelectronics, Computer Architecture, Introduction to Python, Internet of Things

Laboratory Setup: Two laboratories (VLSI Design and Internet of Things) were setup by me in the year 2023 in ICFAI University Tripura.

Invited Talk: 1) Invited talk in the IEI Agartala in the month of July, 2023
2) Invited talk in the TIT Agartala in the month of May, 2024

Industrial Training & work done at M/s.BPL Telecom Pvt. Ltd in the field of Switching Technology & gathered a lot of knowledge in maintenance & troubleshooting of ISDN based digital SIGMA INDX 2K & SIGMA INDX 250 EPABX System w.e.f. 28.12.05 to 28.02.06

PROJECT WORK (M. Tech) : **Microelectro Mechanical System:Design of MEMS Based Pressure Sensorfor wide range of Pressure at Jadavpur University**

PROJECT WORK (B. E.) : **Regulated power supply with current foldback and over voltage protection**

VOCATIONAL TRAINING (B.E.) : **At WEBEL POWER ELECTRONICS LTD.on inverter circuit on UPS.**

COMPUTER SKILL : **Languages known: C, Python, Application softwares like MATLAB, TANNER SPICE and VHDL/Verilog HDL (Xilinx and Modelsim Simulator), Proteus, Scilab, app development using using MIT App Inventor tools, knowledge in IOT and AVR Microcontroller programming**

MICROCONTROLLER KNOWN : **Arduino uno atMega328P, AVR atMega16, Raspberry Pi, Microbit, ESP8266, ESP32**

ACHIEVEMENTS: Got Microchip Educator's Accreditation Certificate in July, 2021
: Got National Scholarship in Secondary Education,
: Got Award from National Science Society & Academic Science Culture & Promotion Society.

: Got IT Merit Recognition Award-2005 from NIIT.
: Got national award for best paper in CCSN-2010 at PIET, Rourkela.

REFERENCES

1) Prof. Dr. Debesh Kumar Das, Dept. of CSE, Jadavpur University, Kolkata, West Bengal.
2) Prof. Hafizur Rahaman, HOD, Dept. of IT, IIEST, Shibpur.

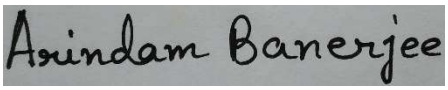
PERSONAL PROFILE

Name: Arindam Banerjee
Date of Birth: 31.12.1981
Father's Name: Ardhendu Banerjee
Sex: Male, Nationality: Indian, Marital Status: Married
Address: Nibedita place, Taki Road, P.O-Barasat,
Pin: 700124

LANGUAGE KNOWN: English (Read and Write), Bengali (Read and Write), Hindi (Speak)

DECLARATION

I do hereby declare that the above mentioned information is correct up to my knowledge & I bear the responsibility for the correctness of the above particulars.



DATE:
PLACE: BARASAT, KOLKATA

ARINDAM BANERJEE