Sushanta Kumar Mandal

CONTACT INFORMATION

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SUMMARY

Experienced Academic Administrator with more than 20+ years of experience in higher education having strong understanding of academic planning, faculty development, strategic planning and quality assurance.

AREA OF EXPERTISE

- Academic Leadership, Strategic Planning, Academic Administration, University Accreditation and ranking, NEP2020, Outcome Based Education, Curriculum Development, Examination and Evaluation, Internal Quality Assurance

Research Area: VLSI Design, Circuit Optimization, Artificial Intelligence, Machine Learning and interdisciplinary research.

PRESENT POSITION **Professor** and **Dean Quality Assurance and Accreditation,** Adamas University, Kolkata, West Bengal.

1. EDUCATION

Degree	University / Institute	Subjects	Year
PhD	School of Information Technology IIT Kharagpur, WB	VLSI Design	2008
MS	Dept. of Electrical Engineering IIT Kharagpur, WB	Electrical Engineering	2002
BE	Jalpaiguri Govt. Engineering College, West Bengal	Electrical Engineering	1993
H.S (10+2)	West Bengal Council of Higher Secondary Education	Science	1988
Madhyamik (10^{th})	West Bengal Board of Secondary Education		1986

4. EMPLOYMENT

INSTITUTION	DESIGNATION	PERIOD	
		FROM	**TO**
Adamas University, Kolkata	Professor and Dean Quality Assurance and Accreditation	01-08-2024	Till date
Adamas University, Kolkata	Professor and Dean Academics, Dean Quality Assurance and Accreditation	08-12-2022	31-07-2024
Brainware University, Kolkata	Professor and Dean, School of Engineering, Director, IQAC	04-08-2022	07-12-2022
Birla Global University, Bhubaneswar, Odisha	**Professor and Dean,** Birla School of Applied Sciences and **Director IQAC**	02-08-2021	30-7-2022
Sharda University, Greater Noida, UP	**Professor**, Department of ECE, Director IQAC and Associate Dean Research	17-12-2018	17-07-2021
Centurion University of Technology and Management, Bhubaneswar, Odisha	**Professor**, Department of ECE, Dean Skill Integrations	01.06.2015	31.10.2018
KIIT University, Bhubaneswar, Odisha	**Professor**, School of Electronics Engineering and Controller of Examinations	05-06-2012	30-11-2014
KIIT University, Bhubaneswar, Odisha	Associate Professor and Associate Dean, School of Electronics Engineering	14-07-2010	04-06-2012
DA-IICT, Gandhinagar, Gujarat	Assistant Professor	22-08-2007	30-06-2010
Asansol Engineering College, Asansol, WB.	Lecturer, Department of Electronics & Communication Engineering	05-07-2002	18-07-2003
Advanced VLSI Design Laboratory, IIT Kharagpur	Research Consultant	04-03-2002	04-07-2002
Sarjana Technovations, Raipur, Chattishgarh	Programming Manager	14-08-2001	28-02-2002

Seemanta Engineering College, Orissa	Lecturer, Department of Electrical Engineering	01-11-1997	19-01-1999

ACADEMIC ADMINISTRATIVE POSITION

- **DEAN ACADEMICS, DEAN QUALITY ASSURANCE & ACCREDITATION, ADAMAS UNIVERSITY**
    - Coordinating academic and co-curricular programs and activities among all 27 Academic Departments under 10 Schools for successful implementation of University's Strategic Plan.
    - Developed framework for NEP2020 UG program and implemented across all schools of Adamas University from Academic Year 2023-24.
    - Implemented student centric learning approaches such as Experiential Learning, Collaborative Learning, participative learning, project based learning, etc.
    - Implemented Outcome Based Education (OBE) curriculum.
    - Course Outcomes (CO) are integrated in the assessment process.
    - Evaluated CO-PO attainment.
    - Revised Examination Regulation of the University in 2023.
    - Implemented Blooms Taxonomy in the assessment process.
    - Continuous monitoring of Mentor-Mentee program to address academics and psychological issues of students.
    - Providing leadership in the development, implementation, monitoring and review of policies, systems and procedures affecting academic matters of the University
    - Receiving, analysing and synthesizing reports from the School Deans for administrative purposes.
    - Managing, monitoring and evaluating the University academic processes.
    - Overseeing academic planning, curriculum development and review of teaching and learning programmes in pursuance of the strategic Planning of the University
    - Chairing and attending University committees and working groups assigned by the Vice Chancellor.
    - Prepared NAAC SSR and submitted on March 2024.
    - Developed and implemented annual Performance Based Appraisal System (PBAS) of the University from 2023 and Career Advancement Scheme (CAS) for faculty promotion from 2023 as per the UGC Regulations.
    - Conducted FDP and seminars regularly on capacity building of faculty.
    - Conducted Academic and Administrative Audit of all Departments.

ACADEMIC AND ADMINISTRATIVE POSITION HELD

- **DEAN, BIRLA SCHOOL OF APPLIED SCIENCES AND DIRECTOR, IQAC, BIRLA GLOBAL UNIVERSITY, BHUBANESWAR, ODISHA**
    - Started new program B.Sc. (Data Science) and developed new curriculum.

- Developed and implement UG & PG curriculum as per NEP 2020 policy from Academic Year 2021-22.
- Design and development of the overall Outcome Based Education (OBE) curriculum.
- NAAC SSR Preparation
- Establishing quality benchmark for various academic and administrative activities of the University.
- Capacity building of faculty and staff on NAAC criteria

- **ASSOCIATE DEAN RESEARCH, SHARDA UNIVERSITY**

  - PhD program coordinator of the university
  - Works closely with all Schools and Departments of the University for research activities
  - Research promotion with in the faculty and staff of the university
  - Improvement in the quality of research and publication
  - Facilitate growth of research activity in the schools
  - Coordinate and plan the development of research ecosystem

- **DIRECTOR, IQAC, SHARDA UNIVERSITY**

  - Gap analysis of all NAAC criteria
  - NAAC SSR preparation under my leadership.
  - Establishing quality benchmark for various academic and administrative activities of the University.
  - Developed and implemented various policies of the University
  - Conducted Academic and administrative audit
  - Performed SWOC analysis of the University
  - Conducted several workshops on different capacity building activities
  - Conducted mock NAAC inspection by experts
  - Achieved QS-iGauge Gold rating for the University
  - Participation in NIRF and ARIIA.

- **DEAN, SKILL INTEGRATIONS, CENTURION UNIVERSITY (OCTOBER 2015 TO OCTOBER 2018)**

  - Developed guidelines for skill courses.
  - Integrated skill-based courses in the under graduate curriculum to enhance employability.
  - Guided faculty members to develop job-oriented skill courses for different programmes of the University.
  - Developed different domain specialized courses as part of curriculum in association with industry partner.
  - Conducted “Surya Mitra” training programme as Head, Centre for Renewable Energy.
  - Developed curriculum for MTech in Renewable Energy.

- **HOD, ECE: CENTURION UNIVERSITY (27-6-2016 TO 27-8-2018)**
    - Prepared and implemented CBCS curriculum.
    - Setting academic strategy of the department in line with University strategic plans and directions and administrative activities of the department
    - Prepared departmental NAAC documentation for the department and University achieved "A" grade in 2015.
    - Prepared documentation for UGC 12B and University got 12B approval.
    - Introduced skill courses in the electronics and communication engineering
    - Established tie-up with Cranes Varsity, Bangaluru for training on Embedded Systems for employability enhancement. More than 80% enrolled students received job offer.
    - Established tie-up with Tessolve Semiconductors, Bangaluru for training on VLSI Design and Verification.
    - Established tie-up with NEMHANS, Bhubaneswar for training on Communication Technologies. All enrolled students received job offer.
    - Established VLSI Design Lab and Embedded System Lab.
    - Conducted several seminars and workshops for staff development.

- **CONTROLLER OF EXAMINATIONS, KIIT UNIVERSITY (08-07-2013 TO 14-11-2014)**
    - Conduction of University End semester examinations for more than 100 programmes in 24 Schools of the University in free and fair manner.
    - Published end semester results within 15 days from the last date of examination earlier it used to take more than one month for result publication.
    - Introduced showing of end semester evaluated answer script to students except medical wing before publication of results. It removes revaluation process.
    - Incorporated more security features in final degree certificates.
- **ASSOCIATE DEAN, ELECTRONICS AND ELECTRICAL ENGINEERING, KIIT UNIVERSITY (06-06-2011 TO 07-07-2013).**
    - In-charge of overall academic activities in the School of Electronics Engineering
    - Developed curriculum for MTech in VLSI Design and Embedded Systems and started MTech in VLSI Design and Embedded Systems in 2011.
    - Established VLSI Design Lab that includes Cadence, Tanner and Xilinx EDA tools.
    - Established Embedded Systems Lab based on ARM processor and FPGA.
    - Revised Digital Electronics Laboratory course experiments.
    - Prepared NBA documentation for ECE & EEE programs.
    - Programme Head of BTech Electronics and Electrical Engineering.
    - MTech programme coordinator for VLSI Design and Embedded Systems

5. SUBJECTS TAUGHT AT POST GRADUATE LEVEL

i) Digital VLSI Circuits
ii) Advanced Digital VLSI Design
iii) Testing of VLSI Circuits
iv) VLSI Design Lab
v) Low Power VLSI Design
vi) FPGA Architecture and Design
vii) Digital System Design using Verilog
viii) Neural Networks
ix) Research Methodology

6. RESEARCH AND PUBLICATIONS

A. THE FOLLOWING M. TECH THESES WERE AWARDED UNDER MY SUPERVISION.

1. "Face Recognition using PCA and ANN algorithm", Swagatika Nayak, 2018
2. "Design and Synthesis of I2C Bus Protocol", Pallavi Pujapanda, 2018
3. "Frequency Reconfigurable Antenna Using Metasurface", Sonalika Satpathy, 2017
4. "Design and Analysis of 6TSRAM Cell using Different Technologies", Subhashree Rath, 2017
5. "Design and Implementation of Low Power High Speed Single Precision Floating Point Multiplier", Manoroma Padhy, 2016
6. "Design and Implementation of Low Power High Speed Wide Multiplier Architecture", Smarika Rout, 2016
7. "Flipped Voltage Follower and its Application in Low Voltage Analog Signal Processing", Amarjyoti Satpathy, 2015
8. "Multi-Threshold CMOS D-Latch based Square Root Carry Select Adder in 45 nm CMOS Process Technology", Adyasa Dash, 2015
9. "High Speed Low Power Current Comparator", Adyasa Rath, 2014
10. "Datapath design using Reversible Logic", L. B. Omprakash, 2014
11. "High Speed Power Efficient Datapath Design using Vedic Mathematics", Suryasnata Tripathy, 2014
12. "Low Power Floating Point Multiplier design", Anindita Das, 2014
13. "High Speed Low Power Analog Circuit Design", Subhrajyoti Das, 2014
14. "Power Efficient CORDIC Design", Adyasa Samantaray, 2014
15. "PLL Design in 45 nm Process", Sweta Padma Dash, 2014
16. "A Low Offset, Fast Settling, Rail-to-Rail, Stable Operational Amplifier in 180 nm Technology", Anindita Das, 2013
17. "FGMOS based low-voltage low-power high output impedance regulated cascode current mirror", Abhinav Anand, 2013
18. "High Speed Low Power Floating Gated SRAM", Pratim Bhattacharya, 2013
19. "A 5 GHz LC Voltage Controlled Oscillator in 90 nm CMOS Technology", Pratik Ganguly, 2013

20. "Design, Modelling and Applications of Interdigital Capacitors (IDCs) to Realize the Metamaterial Characteristics", Samira Priyadarshini Pati, 2012
21. "Design of CMOS Comparator", T K Srinivasa, 2012
22. "High Performance Low Power LC VCO Design", Anindita Sahoo, 2012
23. "FPGA Implementation of Viterbi Decoder", Sangram K. Khandai, 2011
24. "A 6 Bit 800 MHz Time-Interleaved Analog to Digital Converter based on Successive Approximation in 65 nm Standard CMOS Process", Arunkumar Salimath, 2009
25. "Analysis and Modeling of Power Distribution Network and Decoupling Network Design strategies for High Speed Digital and Analog VLSI System", Abhishek Pathak, 2009
26. "BIST Architecture for Mixed-signal Systems", Mahavir Ramlal Jain, 2009
27. "Particle Swarm Optimization Based Synthesis of Analog Circuits using Neural Network Performance Macro models", Neha Saxena, 2009
28. "Design of low voltage high performance voltage controlled oscillator", R. Ramesh, 2008
29. "Designing of an Efficient Power Clock generation circuit for Complementary Pass-transistor Adiabatic Logic Carry Save Multiplier", P. Ranjith, 2008
30. "A High-Speed 512-point FFT Single-Chip Processor Architecture", Ajay Kumar Sinha, 2008

B. PHD THESIS/DISSERTATIONS

Scholars awarded PhD degree under my supervision.

1. "Investigations on Implanted Antennas Inside the Human Body for Biomedical Applications", Medikonda Ashok Kumar, Centurion University, 2018.
2. **"**Macro modeling and Synthesis of Analog Circuits", B. Shivalal Patro, KIIT University, 2018.
3. **"**Design of Low Power High Speed Static Random Access Memory (SRAM) using Floating Gate MOSFET", Kananbala Ray, KIIT University, 2017.
4. "Application of Computational Intelligent Techniques in Electrical System Problems", Jagadish Chandra Pati, KIIT University, 2017.
5. "Analysis of Different Indoor Illumination Methods using Daylight", Badrinarayan Mohapatro, Centurion University, September 2020
6. "Development of Miniaturized Rectenna for Wireless Energy Harvesting", Harish Chandra Mohanta, Deakin University, Australia, June 2021

Students pursuing PhD thesis under my supervision:

1. **"**Low Power SRAM Design using FinFET", Anandita Srivastava
2. "Real-time Facial expression recognition using Machine Learning techniques", Abhilasha Sharma
3. Quality of Healthcare Service: A Comparative Study of Tertiary-Care Public and Private Facilities in West Bengal, India., Anwesha Nag

C. PATENTS

1. **Indian Patent No. 242236 (granted on 19th August 2010)**
   Title: A method of maintaining the zone temperature in a single-zone variable air volume air conditioning (VAVAC)
   Institute: Indian Institute of Technology Kharagpur
   Inventor: Prof. R. C. Arora, Prof. S. Bhattacharyya, Prof. P. K. Das, Prof. A. Patra, Prof. S. Mukhopadhyay and S. K. Mandal

2. **Indian Patent Application No. 202211006902**,
   Date of filing: 09-02-2022,
   Date of Publication: 25-02-2022
   Title of Invention: Cell Capacity Evaluation using Fifth Generation WLAN and IEEE 802.11ax for VBR Traffic.
   Inventors: Dr. Ajay Tiwari, Dr. Vishal Awasthi, Dr. Sushanta Kumar Mandal, Dr. B. Shivalal Patro, Prof.(Dr.) Manish Sharma, Dr. Sahil Thakar

D. REFERRED JOURNAL PAPERS

1. Anandita Srivastav, Usha Tiwari, Sushanta K Mandal, Ashish Sachdeva, A FinFET-Based Low Leakage 10T Static Random Access Memory Cell, Journal of Circuits, Systems and Computers, 13 December 2024
2. Anandita Srivastav, Shailendra Kumar Tripathy, Usha Tiwari and Sushanta K. Mandal, Comprehensive Study of Low-Power SRAM Design Topologies, Recent Advances in Electrical & Electronic Engineering, 31 October, 2023.
3. Rita Sharma and Sushanta K. Mandal, Application of Virtual Reality in Orthopaedic Conditions, Journal of Scientific and Technical Research, 11(1), pp. 29-32, June 2021.
4. Charu Chaudhary, Govind Pandey, Rahul K. Jayas and Sushanta K. Mandal, Review of Health Monitoring System, Indian Journal of Natural Sciences, Vol. 12, Issue 66, pp. 31453-31458, June 2021.
5. Khushboo Kumari and Sushanta K. Mandal, Virtual Reality Application in Neurological Rehabilitation, Journal of Scientific and Technical Research, vol. 10, issue 1&2, pp , December 2020.
6. Harish Chandra Mohanta, Abbas Z. Kouzani, Sushanta K. Mandal, Compact Frequency Reconfigurable Metasurface Antenna, Indian Journal of Natural Sciences, Vol. 59, Issue 10, pp 18352-18359, April 2020.
7. B. N. Mohapatra, M. Ravi Kumar and Sushanta K. Mandal, “Analysis of light tubes in interior daylighting system for building”, Indonesian Journal of Electrical Engineering and Computer Science, Vol. 17, No. 2, pp 710-719, February 2020.
8. Harish Chandra Mohanta, Abbas Z. Kouzani, Sushanta K. Mandal, "Reconfigurable Antennas and Their Applications." Universal Journal of Electrical and Electronic Engineering Vol. 6 (4) pp 239 – 258, September 2019.
9. B. N. Mohapatra, M. Ravi Kumar and Sushanta K. Mandal, “Evaluation of daylight illuminance on the performance of light shelves of an office room”, Journal of Engineering Science and Technology, Vol. 14, No. 4, pp 1984-1999, August 2019.

10. B. N. Mohapatra, M. Ravi Kumar and Sushanta K. Mandal, “Positioning of light shelves to enhance daylight illuminance in office rooms”, Indonesian Journal of Electrical Engineering and Computer Science, Vol. 15, No. 1, pp 168-177, July 2019.
11. Kunja B. Swain, Sushanta K. Mandal, Satya Sopan Mahato and Murthy Cherukuri, “A Brief Review on Fault Detection, Classification and Location on Transmission Lines Using PMUs”, International Journal of Management, Technology and Engineering (IJMTE), vol. 8, issue 12, pp 2609-2617, December 2018.
12. B. N. Mohapatra, M. Ravi Kumar and Sushanta K. Mandal, “Analysis of Daylighting using Daylight Factor and Luminance for Different Room Scenarios”, International Journal of Civil Engineering and Technology (IJCIET), vol.9, no. 10, pp. 949-960, October 2018.
13. A.V.S Swathi, V.V.S.S.S. Chakravarthy and Sushanta K. Mandal, “Review on Multi-objective Optimization of Linear and Circular arrays using Evolutionary Computing Tools”, International Journal for Research in Engineering Application & Management (IJREAM), vol.4, issue-02, pp-543-546, May 2018.
14. B. N. Mohapatra, M. Ravi Kumar, Sushanta K. Mandal and R. K. Mohapatra, “Daylight Factor Analysis with Slat Angle Control for Glare Reduction in a Three Storied Office Building”, International Journal of Applied Engineering Research, vol.13, no. 15, pp. 12040-12046, August 2018.
15. Ch. Laxmi, M. Narendra Kumar and Sushanta K. Mandal, “A Comprehensive Review on Energy Management Strategies in Hybrid Renewable Energy System”, International Journal of Engineering & Technology (UAE), Volume 7, No. 2.23, pp. 450-454, April 2018.
16. Swagatika Nayak and Sushanta Kumar Mandal, "Face recognition using PCA and ANN algorithm", International Journal of Creative Research Thoughts (IJCRT), ISSN:2320-2882, volume.6, issue 2, page no pp.588-594, April-2018.
17. S. Patnaik, K. Parvathi and Sushanta K. Mandal, Efficient and Simplified Adaptive Neuro Fuzzy Based Edge Detection for Digital Image Processing Using ANFIS for Edge Strength, International Journal of Pure and Applied Mathematics, vol. 117, No. 15, pp. 253-261, 2017.
18. Abinash Gaya and Sushanta K. Mandal, Experimental Analysis of a MIMO System using Multiple Antenna Arrays and Estimation of Location Parameters, International Journal of Pure and Applied Mathematics, vol. 114, No. 7, pp. 249-258, 2017.
19. B. S. Patro and Sushanta K. Mandal, Macro-modeling of OTA using ANN for Fast Synthesis, International Journal of Engineering, Science and Mathematics, Vol. 6, Issue 8 (Special Issue), pp. 752-759, December 2017.
20. Harish Chandra Mohanta and Sushanta K. Mandal, Frequency Reconfigurable Antenna using Metasurface of Rectangular Loop Unit Cell, International Journal of Engineering, Science and Mathematics, Vol. 6, Issue 8 (Special Issue), pp. 766-773, December 2017.
21. S. Patnaik, K. Parvathi and Sushanta K. Mandal, Development of Simple Edge Detection Technique using FIS, Journal of Advanced Research in Dynamics and Control Systems, Issue 12-Special, pp. 323-332, 2017.
22. B. S. Patro and Sushanta K. Mandal, Support Vector Machine based Macro-Modelling of Voltage Controlled Oscillator for Fast Synthesis Purpose, Journal of Advanced Research in Dynamics and Control Systems, Issue 12-Special, pp. 355-663, 2017.

23. B. S. Patro and Sushanta K. Mandal, A Multi Output Formulation for Analog Circuits Using MOM-SVM, Indonesian Journal of Electrical Engineering and Computer Science, Vol. 7 (1), pp 90-96, July 2017.
24. J. C. Pati, C. K. Panigrahi and Sushanta K. Mandal, Design Aspects for Optimal Tuning of Controllers by AI Techniques, International Journal of Current Science and Technology (IJCST), vol. 5, No. 2, pp. 376-384, April 28, 2017
25. Kanan Bala Ray, Sushanta K. Mandal and B. S. Patro, Low Power, High speed, Low leakage Floating Gate SRAM Cell using LECTOR Technique, Indian Journal of Science and Technology, Vol. 9 (45), pp.1-6, December 2016.
26. Kanan Bala Ray, Sushanta K. Mandal and B. S. Patro, Low Power FGSRAM Cell Using Sleepy and LECTOR Technique, Indonesian Journal of Electrical Engineering and Computer Science, Vol. 4, No. 2, pp 333-340, November 2016.
27. B. Shivalal Patro and Sushanta K. Mandal, A Novel Modeling Technique for Operational Amplifier Using RBF-ELM, Journal of Engineering Science and Technology Review, 9(4), pp 74-76, September 2016.
28. Medikonda Ashok Kumar, Sushanta K. Mandal and G. S. N. Raju, Serpentine Micro-strip Patch Antennas to Operate in MICS-Band by Using Coaxial Probe Feeding Technique, International Journal of Scientific Engineering and Technology Research, vol. 5, pp., issue-25, 4801-4806, 2016.
29. Smaranika Rout and Sushanta K. Mandal, Implementation of Low Power and High-Speed Single Precession Floating Point Multiplier using Kogge-Stone Adder and Dadda Multiplier, International Journal of VLSI Design and Communication Systems (IJVDCS), vol. 4, issue-9, pp 0668-0674, 2016.
30. Manorama Padhy and Sushanta K. Mandal, Realization of Low Power and High-Speed Wide Multiplier Architecture Using D-Latch and Wallace Tree Multiplier, International Journal of VLSI Design and Communication Systems (IJVDCS), vol. 4, issue-9, pp 0761-0766, 2016.
31. Suryasnata Tripathy, Sushanta K. Mandal, B. Shivalal Patro and L. B. Omprakash, Low Power, High Speed 8-Bit Magnitude Comparator in 45 nm Technology for Signal Processing Application, Indian Journal of Science and Technology, Volume 9, Issue 13, April 2016.
32. Subhrajyoti Das, Sushanta. K. Mandal, Adyasha Rath, Sweta Padma Dash, Low Power High Speed Indirect Frequency Compensated OPAMP with Class AB Output Stage in 180 nm CMOS Process Technology, Intelligent Computing, Communication and Devices, Advances in Intelligent Systems and Computing, Volume 308, pp. 471-478, August 2015, Springer, (ISBN 978-81-322-2011-4).
33. Suryasnata Tripathy and Sushanta K. Mandal, Low Power, High Speed, Low Power Datapath Design using Multi-Threshold Logic in 45 nm Technology for Signal Processing Application, International Journal of Scientific and Engineering Research, Volume 5, Issue 5, pp 17-22, May 2014 (ISSN 2229-5518).
34. Suryasnata Tripathy, L B OM Prakash, B. S. Patro and Sushanta K. Mandal, A Comparative Analysis of Different 8-bit Adder Topologies at 45nm Technology. International Journal of Engineering Research and Technology, Volume. 2. Issue 10, October 2013.

35. Pratim Bhattacharjee, G. L. K. Moganti and Sushanta K. Mandal, *High speed-low leakage-multi threshold 45 nm floating gated SRAM*, International Journal of Engineering Research and Applications (IJERA), Vol. 3, Issue 3, pp.642-645, May-Jun 2013.
36. Abhinav Anand, Sushanta K. Mandal, Anindita Dash and B. Shivalal Patro. *FGMOS based low-voltage low-power high output impedance regulated cascode current mirror*, International Journal of VLSI Design & Communication Systems (VLSICS) Vol.4, No.2, pp. 39-50, April 2013.
37. Sushanta K. Mandal, Shamik Sural and Amit Patra, ANN and PSO based Synthesis of On-Chip Spiral Inductors for RF ICs, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, vol. 27, no.1, pp. 188-192, January 2008.
38. Sushanta K. Mandal**,** Shamik Sural and Amit Patra, Broadband Scalable Model for Si-RF On-Chip Spiral Inductors with Substrate Eddy Current Effect, Wiley Periodicals, Inc. International Journal of RF and Microwave Computer-Aided Engineering 17: 560-573, 2007.

E. BOOK CHAPTERS

1. K Swain, S. S. Mahato, S. K. Mandal, M Cherukuri, Microgrid Situational Awareness Using Micro-PMU - Advances in Smart Grid Automation and Industry 4.0, Lecture Notes in Electrical Engineering, pp.573-580, April 2021, Springer, Singapore.
2. Swain K.B., Mahato S.S., Mandal S.K., Cherukuri M. Real-Time Transmission Line Situational Awareness Using NI Phasor Measurement Unit. In: Advances in Electrical Control and Signal Systems. Lecture Notes in Electrical Engineering, vol 665. pp. 443-454, July 2020, Springer, Singapore
3. B. S. Patro and Sushanta K. Mandal, "Macromodelling of Analog Circuits" in VLSI Design and Testability Issues, CRC Press, Taylor & Francis, August 2020 (In press).
4. Medikonda Ashok Kumar, Sushanta K Mandal and G S N Raju, Implanted Antennas Inside the Human Body: Design, Simulations, and Fabrication. In: Microelectronics, Electromagnetics and Telecommunications, Lecture Notes in Electrical Engineering, Springer, Singapore, vol 471. pp. 609-616, 2018.
5. Medikonda Ashok Kumar, Sushanta K Mandal and G S N Raju "Implanted antennas inside the human body, Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications (ICMEET-2016). Lecture Notes in Electrical Engineering, Springer, vol 434, pp.519-527, 2017.

F. INTERNATIONAL/NATIONAL CONFERENCE/SEMINAR PAPERS:

1. Usha Tiwari, Abhilasha Sharma and Sushanta K Mandal Real-Time Emotion Classification and Prediction Using a Hybrid Facial Expression Recognition Model Emotion Recognition in Human Resources' Future, 27th International Symposium on Wireless Personal Multimedia Communications (WPMC2024), 17-20 November, 2024
2. Khushboo Kumari, Sushanta K. Mandal and Bhuvnesh Kumar, Interhemispheric Inhibition of Human Motor Cortex via Transcranial Direct Current Stimulation and Its Advancement Over Others, National Seminar on Applied Research, (October 21-22, 2021), Sharda University
3. Khushboo Kumari, Sushanta K. Mandal and Bhuvnesh Kumar, Noninvasive Brain Stimulation and It's Maneuvers in Developing Neuroplasticity, National Seminar on

Applied Research, (October 21-22, 2021), Sharda University.

4. Aafreen and Sushanta. K. Mandal, Robot-Assisted Therapy in Improving Upper Extremity Function Among Post Stroke Patients, National Seminar on Applied Research, (October 21-22, 2021), Sharda University.
5. Rita Sharma and Sushanta K. Mandal, The Impact of Frozen Shoulder on Patients' Quality of Life, National Seminar on Applied Research, (October 21-22, 2021), Sharda University.
6. Rita Sharma and Sushanta K. Mandal, Role of Active Release Technique in Improving Trigger Points Around Shoulder Joint, National Seminar on Applied Research, (October 21-22, 2021), Sharda University.
7. Kunjabihari Swain, Satya Sopan Mahato, Sushanta K Mandal and Murthy Cherukuri, Microgrid Situational Awareness Using MicroPMU, International Conference on Emerging Trends for Smart Grid Automation and Industry 4.0, December 5-7, 2019, BIT, Mesra, Ranchi, India.
8. Kunjabihari Swain, Satya Sopan Mahato, Sushanta K Mandal and Murthy Cherukuri, A Brief Review on Fault Detection, Classification and Location on Transmission Lines Using PMUs, International Conference on Management, Sciences, Engineering and Applications (ICMSEA - 2018), December 20-22, 2018, Vizag, India
9. Kunja B. Swain, Piyush D. Pattnaik, Sushanta K. Mandal, and Satya S. Mahato, Design and Optimization of Hybrid Photovoltaic Cell by Converting Thermal Loss to Usable Electric Energy, XIX International Workshop on the Physics of Semiconductor Devices, December 11-15, 2017, New Delhi.
10. B. S. Patro, V. Bandana and Sushanta K. Mandal, A Low Phase Noise Wide Tuning Range CMOS Differential Ring Voltage Controlled Oscillator for Signal Processing, International Conference on Communication, Circuits and Systems (iC^3S-2016), February 6-7, 2016, Bhubaneswar, India.
11. Niladri Ghosh, Kanan Bala Ray, Bijoyendra Chowdhury and Sushanta K. Mandal, Low Power 1-Bit SRAM Architecture Design Using GALEOR Technique, International Conference on Communication, Circuits and Systems (iC^3S-2016), February 6-7, 2016, Bhubaneswar, India.
12. Bijoyendra Chowdhury, Kanan Bala Ray, Niladri Ghosh and Sushanta K. Mandal, Design and Analysis of Low Power, High Speed 3-2 Compressor Architectures in 45 nm Technology, International Conference on Communication, Circuits and Systems (iC^3S-2016), February 6-7, 2016.
13. Amarjyoti Satpathy, Subir Maity and Sushanta K. Mandal, A Flipped Voltage Follower Based Analog Multiplier In 90nm CMOS Process, **IEEE Proceedings** of International Conference on Advances in Computer Engineering and Applications – 2015, IMS Engineering College, 19^{th}-20^{th} March, 2015, India.
14. Adyasa Das, Sushanta K. Mandal and Jitendra K. Das, High Speed Square Root Carry Select Adder Using MTCMOS D-Latch in 45nm Technology, **IEEE Proceedings** of International Conference on Electrical, Electronics, Signals, Communication & Optimization-EESCO, 24^{th} - 25^{th} Jan-2015.
15. Kanan Bala Ray, Sushree Sangita Das and Sushanta K. Mandal, Multi Threshold Floating Gate SRAM in 180 nm Technology, Proceedings of 1^{st} National Conference on Devices and Circuits, National Institute of Science and Technology, Berhampur, Odisha, India, pp. 138-141, 20-21 February, 2015.
16. Kanan Bala Ray, Prangya Parimita Nanda and Sushanta K. Mandal, One Bit-Line Multi-

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20. Suryasnata Tripathy, L B OM Prakash, B. S. Patro and Sushanta K. Mandal, Low Power, High Speed Full Adder Architectures in 45 nm Technology, International Conference on VLSI and Signal Processing (ICVSP 2014), IIT Kharagpur, January 10-12, 2014.
21. Suryasnata Tripathy and Sushanta K. Mandal, Low Power, High Speed, Low Power Datapath Design using Multi-Threshold Logic in 45nm Technology for Signal Processing Application, National Conference on VLSI Signal Processing and Trend Telecommunication, May 9-10, 2014.
22. Anindita Dash, Sushanta. K. Mandal, B. Shivalal Patro and AbhinavAnand, "A Low Offset Fast Settling Rail-to-Rail Stable Operational Amplifier in 180 nm Technology" 2013 **IEEE Conference** on Information and Communication Technologies (ICT-2013), April 11-12, 2013, India**.**
23. B. S. Patro, J. K. Panigrahi and Sushanta K. Mandal, A 6-17 GHz Linear Wide Tuning Range and Low Power Ring Oscillator in 45nm CMOS Process for Electronic Warfare, **IEEE Proceedings** on 2012 International Conference on Communication, Information and Computing Technology (ICCICT), October 19-20, 2012.
24. Samira Priyadarshini Pati, Sushanta K. Mandal, and Sudhakar Sahu, Design, Characterization and Realization of Left-Handed Metamaterial Characteristics of Interdigital Capacitors, International Conference on Communication, Circuits and Systems (iC^{3}S-2012), October 5-7, 2012.
25. Anindita Sahoo, Sushanta K. Mandal, Design of Ultra low power LC-VCO in 45nm Standard CMOS Process, IJCA Proceedings International Conference on Communication, Circuits and Systems (iC^{3}S-2012), October 5-7, 2012.
26. A. Salimath, C. Debnath, K. Chatterjee and Sushanta K. Mandal, *A 6-bit 800MHz TIADC based on Successive Approximation in 65 nm Standard CMOS Process*, Proceedings of the **23rd IEEE/ACM** International Conference on **VLSI Design**, January 3-7, 2010, Bangalore, India, pp. 312-317.
27. A. Pathak, Sushanta K. Mandal, R. Nagpal and R. Malik, Modelling and Analysis of Power-Ground Plane for High Speed VLSI System, **IEEE Proceedings** of IEEE INDICON 2009, December 18-20, 2009, DAIICT, Gandhinagar, Gujarat, pp. 1-4.
28. Sushanta K. Mandal, Ansul Goyel and Ankit Gupta, *Swarm Optimization Based On-Chip Inductor Optimization*, **IEEE Proceedings** of 4th International Conference on Computers and Devices for Communications (CODEC-09), Institute of Radio Physics and Electronics, University of Calcutta, December 14-16, 2009, Kolkata, India, pp. 1-4.

29. P. Ranjith, Sushanta K. Mandal, and D. Nagchoudhuri, An Efficient Power Clock Generation Circuit for Complementary Pass-Transistor Adiabatic Logic Carry-Save Multiplier, **IEEE Proceedings** of 4th International Conference on Computers and Devices for Communications (CODEC-09), Institute of Radio Physics and Electronics, University of Calcutta, December 14-16, 2009, Kolkata, pp.1 -4.
30. Sushanta K. Mandal, *A Comparison of Genetic Algorithm and Particle Swarm Optimization for On-Chip Spiral Inductor Modeling*, in Proceedings of the International Conference on Information Technology, INTL-INFOTECH 2007, March 19-21, 2007, Haldia, India, pp. 629-633.
31. Sushanta K. Mandal, Ashudeb Dutta, and Amit Patra, *Analysis and Characterization of On-Chip Spiral Inductors on Silicon using Electromagnetic Simulator*, in Proceedings of the 3rd International Conference on Computers and Devices for Communications (CODEC-06), Institute of Radio Physics and Electronics, University of Calcutta, December 18-20, 2006, Kolkata, pp. 407-710.
32. Sushanta K. Mandal, Arijit De, Amit Patra and Shamik Sural, *A Wide-band Lumped Element Compact CAD Model of Si-Based Planar Spiral Inductor for RFIC Design*, in Proceedings of the **19th IEEE/ACM** International Conference on **VLSI Design**, January 3-7, 2006, Hyderabad, India, pp. 619-624.
33. Sushanta K. Mandal, and Arijit De, *A 20GHz Compact Scalable Model of Silicon-based On-Chip Spiral Inductor for RFICs*, in **IEEE Proceedings** of the 15th International Crimean Conference "Microwave and Telecommunication Technology" (CriMico'2005), September 12-16, 2005, Sevastopol, Crimea, Ukraine, Volume-2, pp. 543-546.
34. Sushanta K. Mandal, *Clustering Techniques for Analysis of Large Datasets*, in Proceedings of the International Conference on Reliability and Safety Engineering (INCRESE), December 21-23, 2005, IIT Kharagpur, India, pp.759-773.
35. Sushanta K. Mandal, Arijit De, Amit Patra, and Shamik Sural, *A Simple Wide-Band Compact Model and Parameter Extraction using Particle Swarm Optimization of On-Chip Spiral Inductors for Silicon RFICs*, in **Proceedings of the ACM** Great Lakes Symposium on VLSI, April 17–19, 2005, Chicago, Illinois, USA, pp. 168-171.
36. Arijit De, and Sushanta K. Mandal, *Compact Wide-Band Modelling of Spiral Inductors for RFICs using Particle Swarm Optimization*, in **Proceedings of URSI** GA 2005, Oct. 23–29, 2005, New Delhi, India.
37. Sushanta K. Mandal, Arijit De, Amit Patra, Shamik Sural and T. K. Bhattacharya, *Particle Swarm Optimization and Parameter Extraction of On-Chip Spiral Inductors for RFICs*, in **IEEE Proceedings** of the IEEE India Annual Conference 2004, INDICON 2004, IIT Kharagpur, India, pp. 17-22.
38. Santosh Biswas, Sushanta K. Mandal and Tapan Pattanayak, *Automatic Test System for Testing VLSI Circuits*, in Proceedings of 26th National Systems Conference (NSC), November 18-19, 2002, Hyderabad, India (page 1-13).
39. S. K. Mandal, S. Mukhopadhayay, A. Patra, S. Bhattacharyya, P. K. Das and R. C. Arora, *Modeling and Closed-loop Simulation of a Variable Air Volume Air Conditioning System*, in Proceedings of International Conference on Energy Automation and Information Technology (EAIT), December 10-12, 2001, IIT Kharagpur, India, pp. 812-817.
40. B. Das, A. Patra, S. Mukhopadhayay, S. K. Mandal, and S. De, *Fault-tolerant control of Variable Air Volume Air Conditioning Systems using Sensor Validation via Artificial Neural Networks*, in Proceedings of International Conference on Energy Automation and Information Technology (EAIT), December 10-12, 2001, IIT Kharagpur, India, pp. 802-

807.

41. A. G. Thosar, B. A. van Wermeskerken, S. K. Mandal, A. Patra, S. Mukhopadhayay, R. C. Arora, S. Bhattacharyay and P. K. Das, *Energy Optimizing Control of a Variable Air Volume Air Conditioning System*, in Proceedings of International Conference on Energy Automation and Information Technology (EAIT), December 10-12, 2001, IIT Kharagpur, India, pp. 818-823.

7. SEMINAR/WORKSHOP ATTENDED

1. One-week online Faculty Development Programme on "Human Values and Ethics", Organized by Sharda University, Greater Noida, UP, India, 6-11 July, 2020.
2. Virtual National Conference on “COVID-19 and Higher Education: Challenges and Responses”, organized by Internal Quality Assurance Cell, Sharda University, Greater Noida, on 2 - 3 June 2020.
3. "Online Learning Workshop for Faculty: Preparing for Online Learning; Engaging for Online Learning; Evaluating and Assessing Students for Online Learning" April 1-3, 2020, organized by QASPIR, UK in collaboration with Association of Indian Universities.
4. National Conference on "Empowering Students to be Industry Ready & How to Select Right Career Path" organized by Panasonic India Innovation Centre and CMAI Association of India, Jan 28, 2020, Vigyan Bhavan, New Delhi.
5. International Conference on Mathematical Sciences in Engineering Applications (ICMSEA - 2017), December 22-24, 2017 at Visakhapatnam, Andhra Pradesh, India.
6. Faculty Development Programme on Solar Photovoltaic Systems, June 27-30, 2017, organized by Centre for Renewable Energy and Environment, CUTM, Bhubaneswar.
7. National Conference on Device and Circuits, Feb 20-21, 2015, organized by NIST, Brahmapur, Odisha
8. National Conference on VLSI Signal Processing and Trend in Telecommunication, May 9-10, 2014, organized by Department of Electronics & Telecommunication Engineering, C. V. Raman College of Engineering, Bhubaneswar, Bhubaneswar, Odisha.
9. Two days NBA Training for Master Trainer’s/Evaluators at Suresh Gyan Vihar University, Jaipur on 18th & 19th February, 2013, organized by NBA, India.
10. Workshop on “Solar Energy – The Future” February 18, 2012, KIIT University.
11. Two-days’ Workshop on Soft computing and Optimization Techniques, April 9-10, 2011, KIIT University
12. IEEE/ACM International Conference on VLSI Design, January 3-7, 2010, Bangalore, India
13. IEEE INDICON 2009, December 18-20, 2009
14. National workshop on PhD Research in VLSI, DA-IICT, Gandhinagar, January 11, 2009.
15. Five Days Mission10X Workshop at Nirma University, 2009.
16. IEEE/ACM International Conference on VLSI Design, 2006, Hyderabad, India
17. International Conference on Computers and Devices for Communications (CODEC), 2006, Kolkata, India
18. IEEE/ACM International Conference on VLSI Design, 2005, Kolkata, India

8. Seminar/Workshop Organized

1. Convener, FDP on Revised NAAC Framework, June 26-30, 2023, Adamas University.
2. Convener, Faculty Development Program on Entrepreneurship Development, February 21, 2023, Adamas University.
3. Convener, One-week Faculty Development Programme on Research Methodology, April 05-09, 2021, Sharda University.
4. Coordinator, Faculty Development Programme on Solar Photovoltaic Systems, June 27-30, 2017, organized by Centre for Renewable Energy and Environment CUTM, Bhubaneswar
5. Organizing Chair, 2nd National Conference on Mechatronics, Computing & Signal Processing, CUTM Bhubaneswar, April 7, 2017.
6. General Chair, IEEE Electron Devices Society Bhubaneswar Kolkata Mini Colloquium on Advanced Electron Devices and Circuits, KIIT University, 3rd-4th December 2014.
7. Convener, International Conference on Communication, Circuits and Systems (iC^{3}S-2012), October 5-7, 2012, KIIT University, Bhubaneswar, Odisha, India.
8. Organizing Member, Two days' Workshop on Soft computing and Optimization Techniques, April 9-10, 2011, KIIT University
9. Organizing Member, IEEE INDICON 2009, December 18-20, 2009
10. Organizing Member, National workshop on PhD Research in VLSI, DA-IICT, Gandhinagar, January 11, 2009.

9. INVITED LECTURE/SESSION CHAIR

1. Delivered lecture on "Revised NAAC Criteria" in the FDP on Revised NAAC Framework, Adamas University, June 26-30, 2023.
2. Delivered invited talk on "Research Types and Problem Identification" in the 6-Day Faculty Development Programme on Application of Research Tools & Techniques, Sharda University, April 31- June 05, 2021.
3. Delivered invited talk on "Writing and publication of research paper" How to write", in the One-week Faculty Development Programme on Research Methodology, Sharda University, April 05-09, 2021.
4. Delivered invited talk on "IoT based Remote Health Monitoring System", in the International Conference on Applied Sciences and Engineering (ICIRASE-2021), Roorkee Institute of Technology, February 20-21, 2021.
5. Delivered full-day hands-on session on "Neural Network and Deep Learning using MATLAB" in the Three Days Workshop on "Practical Aspects of MATLAB" organized by Dept. of ECE, Sharda University, March 25-27, 2019.
6. Chaired a session at International Conference on Mathematical Sciences in Engineering Applications (ICMSEA - 2017), December 22-24, 2017 at Visakhapatnam, Andhra Pradesh, India.
7. Delivered invited talk on "On-Chip Spiral Inductor Overview and Design" at Faculty Development Programme on "Recent Trends on VLSI Design & Embedded Systems" organized by the Department of Electronics & Telecommunication Engineering, C. V. Raman College of Engineering, Bhubaneswar during 26th July to 28th July 2012

8. Chaired a session on "Engineering Sciences" at 99th Indian Science Congress 2012, KIIT University.
9. Delivered invited lecture on "Full Custom VLSI Design Flow" at Staff Development Program on "Recent Trends in Medical Imaging using VLSI" December 19-31, 2011, OEC, Bhubaneswar, India.
10. Delivered invited talk on "Neural Network modeling of integrated inductors" at Two-day Workshop on "Soft computing and Optimization Techniques", April 9-10, 2011, KIIT University.
11. Delivered invited talk at NUCON 2009 Nirma University, Ahmedabad, Gujarat.
12. Delivered invited lecture on Advanced Digital VLSI Design at STTP 2010, Nirma University, Ahmedabad, Gujarat

10. REFEREE/ASSESSOR/PROGRAMME COMMITTEE MEMBER

1. Assessor of NPTEL Course "Design Verification and Test of Digital VLSI Circuits"
2. Referee of International Journal of RF and Microwave Computer-Aided Engineering, John Wiley & Sons.
3. Referee of IET Journal Circuits, Devices & Systems
4. Referee of Design, Automation and Test in Europe (DATE) 2008
5. Referee of Design Automation Conference (DAC) 2008, 2009
6. Referee of INDICON 2009
7. Referee of IC3S-2012
8. Technical Programme Committee member of VDAT-2016, 2017, 2018, 2019,2020
9. Referee of Silicon (Springer – Nature)
10. Assessor of AICTE Quality Improvement Scheme (AQIS) STTP (2018-19)
11. Assessor of PhD theses of various universities
12. Expert, Faculty recruitment committee of different technical institutions.
13. Member of Technical Programme Committee, 3rd International Conference of Computational Intelligence and Networks (CINE), 2017, KIIT University
14. Member of Technical Programme Committee, 2nd International Conference of Computational Intelligence and Networks (CINE), 2016, KIIT University

11. MEMBER IN PROFESSIONAL BODIES AND INSTITUTIONS

Member, IEEE
Life Member, Indian Society of Systems for Science & Engineering (ISSE)
Member, Board of Studies, ECE, SET, Adamas University
Member, Academic Council, Adamas University
Member, IQAC, Adamas University
Member, Board of Research, Adamas University
Member, Board of Studies, EEE, DRIEMS, Cuttack
Member, Board of Studies, EE, MAKAUT, West Bengal